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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,925	03/06/2002	Kazuto Nishimura	FUJY 19.478	7074

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EXAMINER	
WONG, WARNER	
ART UNIT	**PAPER NUMBER**
2616	
MAIL DATE	**DELIVERY MODE**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/091,925	NISHIMURA ET AL.	
	Examiner	Art Unit	
	Warner Wong	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7-12 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7-12 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mekkittikul (2005/0249128) in view of Thodiyil (US 6,956,818) and Umayabashi (US 2002/0024971)

Regarding claim 1, Mekkittikul describes:

a node (fig. 3, MPS switch #304) in a ring network system in which a plurality of insertion nodes are connected in loop through a ring transmission path (fig. 3, and where the packets are inserted into the ring transmission path), comprising:

an every-insertion-node oriented buffer unit having individual buffer memories at which arrived packets are inserted into said ring transmission path, and accumulating the packets in said individual memory buffer (fig. 3, each node comprises a collective buffer having individual buffer memories 311-313 each accumulating packets from a particular computer 308-310 to their respective destination computer 319-321, to be inserted to said transmission ring);

a read control unit reading the packets in a fair way on the basis of predetermined weights respectively from individual buffer memories (paragraphs 42-44,

where the buffer controllers 314-316 is the read control unit, and the fair bandwidth allocation scheme evaluates on the basis of predetermined/allocated weights w[i]);

wherein the read control unit implements a weighted read control of the packets stored in the every-insertion-node oriented buffer unit based on weight values (paragraphs 42-44, the buffer controller 314-316 (read control unit) controls the flow in each buffer 311-313 based on weights assigned to the flows).

Mekkittikul fails to describe:

a storage module stored with mappings between said insertion nodes and their respective weight values different from each other as the predetermined weights that are proportional to the number of connections for inserting the packets.

Thodiyil describes:

a storage module stored with mappings between said insertion nodes and weight values different from each other as the predetermined weights are dynamically updated to indicate proportion of the bandwidth or a maximum amount of data to be scheduled for transmission/insertion (abstract, col. 6, lines 51-55 & col. 7, lines 36-40, the arbiter 110 (storage module) stores mappings of each different weight of corresponding cache/queue holding packets inserted from a particular application/computer).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to modify Mekkittikul to incorporate a storage module to store mappings of proportional weights to the corresponding insertion nodes as in the configuration of Thodiyil.

The motivation for combining the teachings is that such added configuration element allows for dynamic alteration of priorities to the different classes of data to be transmitted (Thodiyil, col. 2, lines 14-17).

Mekkittikul and Thodiyil combined describe that the predetermined weights are proportional to the bandwidth, but fail to explicitly describe:

the predetermined weights are proportional to the number of connections for inserting the packets.

However, it would have been obvious to one with ordinary skill of art at the time of invention by applicant to interpret the Thodiyil invention wherein "the predetermined weights are proportional to the maximum amount of data scheduled for transmission" (abstract) suggests that the predetermined weights are proportional to the number of connections for inserting the packets because: in packet switching, each packet sent to a destination represents a connection instance; hence, the more weighted packets are being transmitted more often, equating to a larger number of connection instances.

The motivation for the above suggestion is that it allows higher priority packets to be compensated by sending more to their destinations.

Umayabashi describes a method/insertion node (fig. 3, node 140 with the fairness guarantee/high efficiency hybrid time slot assignment control (FG/HE HTSAC) module 341) which insert arrived packets to the transmission line 191 using the fairness criteria (weight) proportional to the number of connections of the input to the transmission line (paragraph 45-46).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to use the number of connections to the transmission path as the criterion/weight in assigning/scheduling transmission as in Umayabashi for the weight assignment/transmission scheduling of Mekkittikul.

The motivation for combining the teaching is that it allows a plurality of connections to be to be dynamically and fairly assigned for transmission using the bandwidths of a shared transmission line (Umayabashi, paragraph 17).

Regarding claim 11, Mekkittikul describes a packet control method, comprising:

a ring network system in which a plurality of insertion nodes are connected in loop through a ring transmission path (fig. 3).

individual buffer memories at which arrived packets are inserted into said ring transmission path, and accumulating the packets in said individual buffer memories (fig. 3, where the node buffer comprising individual buffer memories 311-313 accumulating packets arrive to the node to be inserted to said transmission ring);

reading the packets in a fair way on the basis of predetermined weights respectively from said individual buffer memories (paragraphs 42-44, where the buffer controllers 314-316 uses a fair bandwidth allocation scheme to evaluate transmission packet flows on the basis of predetermined/allocated weights w[i]).

Mekkittikul fails to describe:

storing mappings between said insertion nodes and weight values different from each other as the predetermined weights that are proportional to the number of connections.

Thodiyil describes:

storing mappings between said insertion nodes and weight values different from each other as the predetermined weights are dynamically updated to indicate proportion of the bandwidth or a maximum amount of data to be scheduled for transmission/insertion (abstract, col. 6, lines 51-55 & col. 7, lines 36-40, the arbiter 110 (storage module) stores mappings of each different weight of corresponding cache/queue holding packets inserted from a particular application/computer).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to modify Mekkittikul to incorporate a storage module to store mappings of proportional weights to the corresponding insertion nodes as in the configuration of Thodiyil.

The motivation for combining the teachings is that such added configuration element allows for dynamic alteration of priorities to the different classes of data to be transmitted (Thodiyil, col. 2, lines 14-17).

Mekkittikul and Thodiyil combined fail to explicitly describe:

the predetermined weights are proportional to the number of connections for inserting the packets.

However, it would have been obvious to one with ordinary skill of art at the time of invention by applicant to interpret the Thodiyil invention wherein "the predetermined weights are proportional to the maximum amount of data scheduled for transmission" (abstract) suggests that the predetermined weights are proportional to the number of connections for inserting the packets because: in packet switching, each packet sent to

a destination represents a connection instance; hence, the more weighted packets are being transmitted more often, equating to a larger number of connection instances.

The motivation for the above suggestion is that it allows higher priority packets to be compensated by sending more to their destinations.

2. Claims 2-4, 6-7, 9-10 and 12-14, 16-17 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mekkittikul in view of Umayabashi and Thodiyil as applied to claims 1 and 11 above respectively, and further in view of Kilkki (6,219,351).

Regarding claims 2 and 12, Mekkittikul and Thodiyil combined fail to explicitly describe:

an identifying unit identifying said insertion node at which the packets are inserted into said ring transmission path on the basis of specifying information contained in the packet;

an accumulation control unit (fig. 6, BMs) accumulating the packets in the corresponding every-buffer memory on the basis of a result of identifying said insertion node.

Kilkki describes:

an identifying unit identifying said insertion node at which the packets are inserted into said ring transmission path on the basis of specifying information contained in the packet (INW switch of fig. 6 and col. 5, lines 22-23, where the INW

switches/identifies packets destined for a particular output/insertion node on the basis of the routing tag).

an accumulation control unit (fig. 6, BMs) accumulating the packets in the corresponding buffer memory (fig. 6, OBF[1..n]) on the basis of a result of identifying said insertion node (fig. 6 and col. 5, lines 22-23, after INW switches/identifies the destination/output port of the packet).

It would have been obvious to one with ordinary skills in the art at the time of invention by applicant to deploy the buffering used by Kilkki into the combined node of Mekkittikul and Thodiyil.

The motivation being that "the switch must have buffering capacity to avoid the necessity of discarding cells in such a situation", (Kilkki, col. 2, lines 8-10).

Regarding claims 7 and 17, Mekkittikul, Thodiyil and Kilkki combined describe all limitations set forth in claims 2 and 12 respectively.

Mekkittikul further describes:

buffer memory of said every-insertion-node oriented buffer unit (Mekkittikul, fig. 3, #322-324 & #304) is physically segmented into a plurality of areas (Mekkittikul, paragraph 42, "Each of these computers 308-310 has a corresponding [separate] buffer 311-313);

said accumulation control unit (Mekkittikul's input to individual buffers 311-313) permits only the packet from said corresponding insertion node to be written to each of the segmented areas of the buffer memory (Mekkittikul, fig. 3, #322-#324 and

paragraph 42, where only the personal computer/user may insert packets to the its corresponding buffer).

Regarding claims 9 and 19, Mekkittikul, Thodiyil and Kilkki combined describe all limitations set forth in claims 2 and 12 respectively.

Kilkki further describes: the identifying unit (switch) identifies said insertion node at which the packet is inserted into said ring transmission path on the basis of an insertion node number (routing tag) as the specifying information contained in the packet (col. 5, lines 22-23, where the switch identifies the destination by the routing tag of the cell.)

It would have been obvious to one with ordinary skills in the art at the time of invention by applicant to deploy the buffering used by Kilkki into the combined node/method of Mekkittikul and Thodiyil.

The motivation being that "the switch must have buffering capacity to avoid the necessity of discarding cells in such a situation", (Kilkki, col. 2, lines 8-10).

Regarding claims 10 and 20, Mekkittikul, Thodiyil and Kilkki combined describe all limitations set forth in claims 2 and 12 respectively.

Kilkki further describes: a storage module (fig. 6, table) stored with mapping between traffic identifiers of the packets (fig. 6, VPI/VCI) and the insertion node numbers (fig. 6, routing tags) and wherein said identifying unit (switch) identifying said insertion node at which the packet is inserted into said ring transmission path on the basis of the insertion node number corresponding to the traffic identifier, as the specifying information contained in the packet (col. 5, lines 22-23, where the switch

identifies the destination by the routing tag of the cell), which is obtained by referring to said storage module (col. 5, lines 18-21).

It would have been obvious to one with ordinary skills in the art at the time of invention by applicant to deploy the buffering used by Kilkki into the combined node of Mekkittikul and Thodiyil.

The motivation being that "the switch must have buffering capacity to avoid the necessity of discarding cells in such a situation", (Kilkki, col. 2, lines 8-10).

3. **Claims 8 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mekkittikul in view of Thodiyil, Umayabashi and Kilkki as applied to claims 2 and 12 above respectively, and further in view of Mansour (2003/0067931).

Mekkittikul, Thodiyil and Kilkki combined describe:

Individual buffer memories of said every-insertion-node oriented buffer unit (Mekkittikul, fig. 3, #322-324) are physically segmented into a plurality of areas (Mekkittikul, paragraph 42, "Each of these computers 308-310 has a corresponding [separate] buffer 311-313), and

said accumulation control unit writes the packet from said corresponding insertion node to each of the individual buffer memories (Mekkittikul, fig. 3, #322-#324 and paragraph 42, where only the personal computer/user may insert packets to the its corresponding buffer).

Mekkittikul, Thodiyil and Kilkki combined fail to explicitly describe:

individual buffer memories in which the shared storage areas is dynamically logically segmented.

Mansour explicitly describes:

individual buffer memories in which the shared storage areas is dynamically logically segmented (fig. 1, # memory and paragraph 4, "Once inside the memory, packets are organized into separate output queues, one queue for each output line").

It would have been obvious to one with ordinary skill in the art at the time of rejection by applicant to use a shared memory and logically segment it for storage areas instead of having physically separated storage areas.

The motivation for combining the teachings is that in using one physical shared memory the design may be more economical in design than in using a multiplicity of physical memory.

Response to Arguments

4. Applicant's arguments with respect to independent claims 1 and 11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Oba (US 6,262,986) describing a packet scheduling scheme capable of realizing a fair scheduling.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Warner Wong whose telephone number is 571-272-8197. The examiner can normally be reached on 6:30AM - 3:00PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on 571-272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Warner Wong
Examiner
Art Unit 2616

WW

KWANG BIN YAO
SUPERVISORY PATENT EXAMINER